Numerical study of energy capability of Si/SiC LDMOSFETs

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Abstract. A comparable study is made on the energy capability of 190 V LDMOSFETs in Si/SiC, SOI, PSOI and PSOSiC technology, using capacitive and inductive switching circuits established in SILVACO Mixed-mode simulators. The results show that the PSOSiC has a thermal advantage compared with other SOI structures under a 48-μs-power-pulse condition, but the Si/SiC device offers superior cooling and energy handling ability in all switching cases despite having a larger chip area.

Introduction

Energy capability is one important parameter in power LDMOSFETs besides specific on-resistance and breakdown voltage [1]. In some circuits where capacitive or inductive loads are present, power transistors can be shorted briefly with simultaneous occurrences of high current and voltage. Therefore, considerable power is produced and the success in handling it will prevent overheating, thereby increasing reliability. Si-on-semi insulating (SI) SiC substrates (Si/SiC) are helpful in these cases, as the underlying SI SiC offers good electrical isolation and high thermal conduction.

Recent progress in the development of Si/SiC devices [2, 3] shows that the quality of the Si on SiC can be similar to those of the SOI and even bulk Si, with appreciable improvement in self-heating. However, the SI SiC platform fails to provide a strong 2D RESURF effect for LDMOSFETs, leading to a reduced blocking voltage [3] and an increased electrical resistance [4] when compared with an equivalent SOI. It can be found that there is a trade-off between electrical and thermal resistance in the thin-film Si/ (SI) SiC transistors using 2D RESURF techniques. Both resistances are important and should be considered in device development. F. Udrea et al. proposed a novel PSOI structure using a p-type SiC as a substrate instead of Si [5]. This configuration offers a P-N RESURF action, a heat conduction path and more importantly, a Si/SiO_2 interface that is better studied than the Si/SiC [5]. As a result, it is interesting to see how this partial Si/SiO_2/SiC architecture (PSOSiC) behaves thermally in contrast with the Si/SiC when driving a capacitive or inductive load.

In this paper, electro-thermal modelling is performed using SILVACO Mixed-mode software package for 190 V LDMOSFETs in SOI, Partial-SOI (PSOI), PSOSiC and Si/SiC technology. Comparisons between them are carried out based upon a capacitive and clamped inductive switching (CIS) circuit, focusing on transient heating under differing power pulse conditions.

Simulated structures

Fig. 1 illustrates a 190 V Si/SiC LDMOS and an equivalent structure modularised for the SOI, PSOI and PSOSiC, created in SILVACO according to [6-8]. The interface charges of Si/SiO_2 and Si/SiC are set to $+4\times10^{10}$ cm^{-2} [9] and -2×10^{10} cm^{-2} [10], respectively. Their threshold voltages are very similar due to their common channel region layout. The differences among the SOI, PSOI and PSOSiC are the materials used in a substrate region, and a region enclosed by dash lines (see Fig.1 left). The PSOI and PSOSiC employ N-type Si and SiC respectively as the substrate material, and both feature a thermal path created by using Aluminum for the region highlighted by dash lines. In

the SOI case, the heat transfer ability of this region is suppressed by using SiO_2, with N-type Si selected for the substrate. This positioning of an opening in the PSOI and PSOSiC minimises the effect of the interrupted buried oxide (BOX) on the SOI RESURF in the transistors and prevents the formation of P-N RESURF mentioned by [5], in a way that a fair comparison among the devices can be achieved. This also reduces the difficulty in fabricating such LDMOSFETs, as the thermally conductive region can be engineered after the wafer bonding processes [7, 8]. However, doing so requires extra chip area [7], unlike the PSOI type having an opening right underneath the active region [5]. In this work, the drift region of the Si/ (SI) SiC device is 12 µm long and 0.6 µm thick, sandwiched between a 1 µm thick field oxide (FOX) and 300 µm thick substrate (see Fig. 1). The same settings apply to the SOI devices simulated, where the thickness of the BOX and the width of the heat conducting region are set to 1 µm and 5 µm respectively. Due to a double RESURF effect induced by the FOX and BOX, the SOI group has a linear doped drift region with a dose twice that of the Si/SiC [4, 6] to obtain the same 190 V breakdown voltage. This results in lower electrical resistance in the devices having the BOX, as can be seen in Fig. 2. Heat conductivity and capacity are specified for each material, considering their relationships with temperature. The substrate terminals of all transistors are grounded and defined as thermal contacts at 300 K.

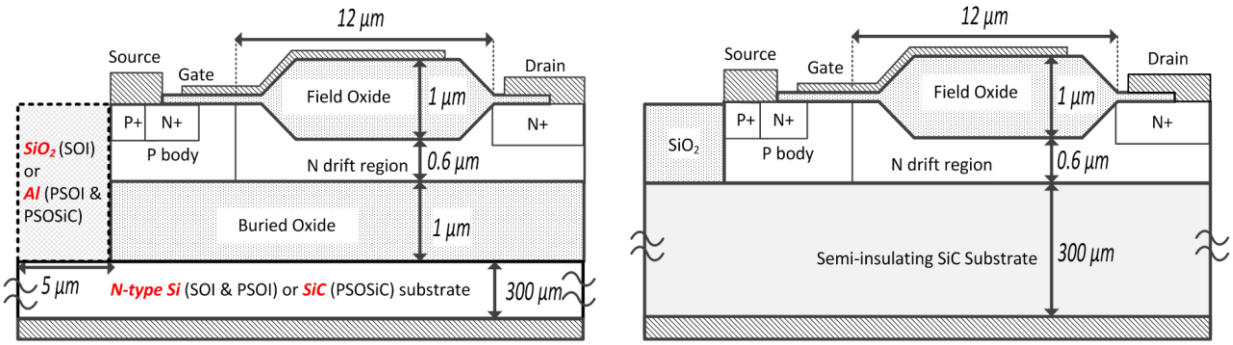

Fig.1. The simulated Si/SiC LDMOS transistor (right) and a universal structure for the SOI, PSOI and PSOSiC (left), where their differences are highlighted.

Results and Discussion

I-V characteristics. Fig.2 shows the electrical behaviour of the transistors in the on- and off-state at 300 K. Self-heating models are deactivated in these simulations and the gate contacts are biased at 12 V for the on-state. The application of SOI RESURF enables them to support a breakdown voltage of 190 V [6], but a higher on-resistance is found in the Si/SiC compared with the SOI group, owing to the absence of the BOX. Negligible difference in the I-V curves is observed among the SOI group members, indicating that the heat conduction path does not affect a device's electrical functioning under isothermal conditions. In the following switching simulations, the device widths of the Si/SiC and other SOI transistors are 1.75 mm and 1 mm respectively in order to achieve the same resistance. Self-heating models are activated.

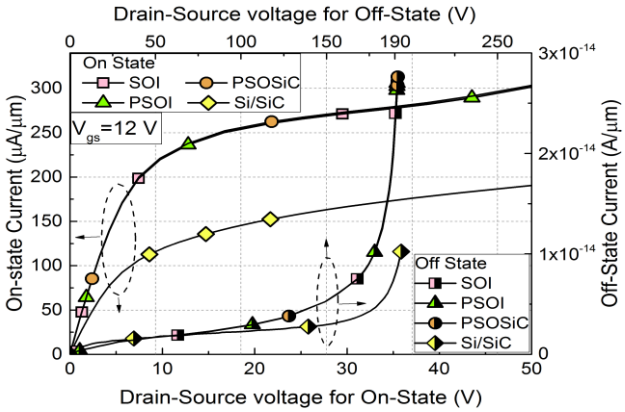

Fig.2 On and off-state IV curves for the simulated devices at 300 K

Capacitive load switching. Fig.3 presents the electrical and thermal results of the devices under capacitor load configurations. The simulated circuit, represented in the inset of Fig.3, is based upon [11], consisting of a 1 kΩ gate resistor, a 12 V pulse signal, a 175 pF capacitor and a 100 kΩ resistor in series with the transistor and a 100 V voltage source. When the device is switched on, a large current is visible initially as a result of capacitor discharge, and lasts for about 70 ns before

the circuit reaches the steady state, with its current being limited to a very low value due to the 100 kΩ series resistor. This can be seen in all the transistors, and a small disparity between the Si/SiC and other counterparts is perceptible as they have differing device width, electrical capacitance and Kirk effect [11]. As a result, their dissipated energy (0.87 µJ) and the shapes of power are similar (see Fig. 3), but the thermal advantage is only found in the Si/SiC while the other solutions are identical regarding temperature rise.

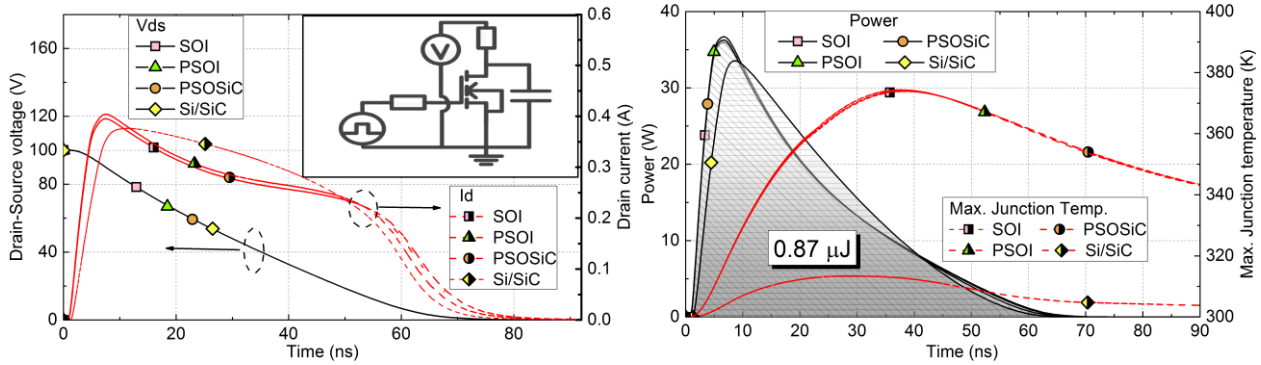

Fig.3. The simulated circuit and I-V switching behaviours for all devices during capacitor's discharge (left), as well as their corresponding power curves and temperature responses (right).

Inductive load switching. The CIS circuit based upon [12] and the resulting devices' electrical characteristics are demonstrated in Fig. 4. The LDMOSFET is controlled by a pulse signal of 12 V and protected by a Zener diode having a breakdown voltage of 150 V. A 5 mH inductor is connected between the transistor and a voltage source of 50 V. This inductor is charged for 10 µs and LDMOS turned off, which triggers the Zener diode conducing current to the ground via a 3 kΩ resistor (R1). Therefore, a voltage is dropped across this resistor, partially switching on the device throughout the inductor discharge period.

As can be seen in Fig. 4, there is no difference among the electrical behaviour of the devices, resulting in the same power pulses 4.8-µs-long with 34 µJ energy, seen in Fig. 5 (left). Similar to the capacitive switching, the Si/SiC has the best thermal performance and the SOI group experiences a rapid temperature increase, but slight deviations among their curves are noticeable and indicative of the effects of the PSOI layout and SiC substrate. This thermal improvement becomes more obvious when the 34 µJ power pulses are reshaped to about 48 µs, by increasing the inductor value and charge time to 500 mH and 100 µs (see Fig. 5 right). The difference at the peak of the maximum junction temperature between the SOI and PSOSiC is about 9 K in this case, greater than 4 K in the previous with the shorter power pulse.

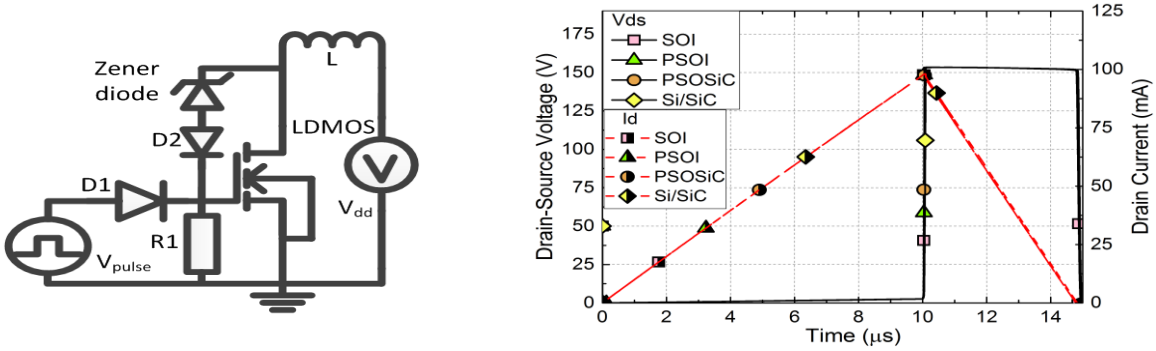

Fig.4. The clamped inductive circuit (left) and the resulting V_{ds} and I_d curves under the conditions of V_{pulse} = 12 V, V_{dd} = 50 V, L = 5 mH, BV_{Zener} = 150 V, R1 = 3 kΩ and a ramp-up time of 10 µs (right).

It has been found that in spite of having a chip area 75% larger than the SOI structure, the Si/SiC solution undergoes negligible heating in any of the switching conditions simulated, exhibiting a very high energy capability. By contrast, the 22% area increase in the PSOSiC does not considerably change the way how energy is handled. This is in part because the thin Si layer offers a weak lateral thermal path which is part of the thermal shunt network. Therefore, the initial

thermal process is mainly heat storage rather than heat transfer, and the thin film again exacerbates the situation by its small heat capacity that induces rapid temperature rise. After a couple of microseconds, this thermal charging of the Si layer is almost complete and the following energy tends to be directed to other regions. The contribution of the added thermal path and the SiC substrate becomes apparent at longer pulse lengths, as can be seen in Fig. 4 and 5. This is similar to the results by L. Yan et al. [7], showing that the thermal impedance of their PSOI devices is the same as that of the SOI at high frequency (10^5~10^6 Hz), but with 30% reduction at low frequency (~10^2 Hz). In the Si/SiC LDMOS, the absence of a BOX minimises the thermal storage within the Si, while the presence of the thin Si film reduces the involvement of Si in thermal conduction. The influence of the SiC substrate is therefore maximised, significantly enhancing heat transfer, while less energy is absorbed in the Si layer. As a result, a fast cooling is achieved even with very short power pulses, which is beneficial to high frequency and power operations.

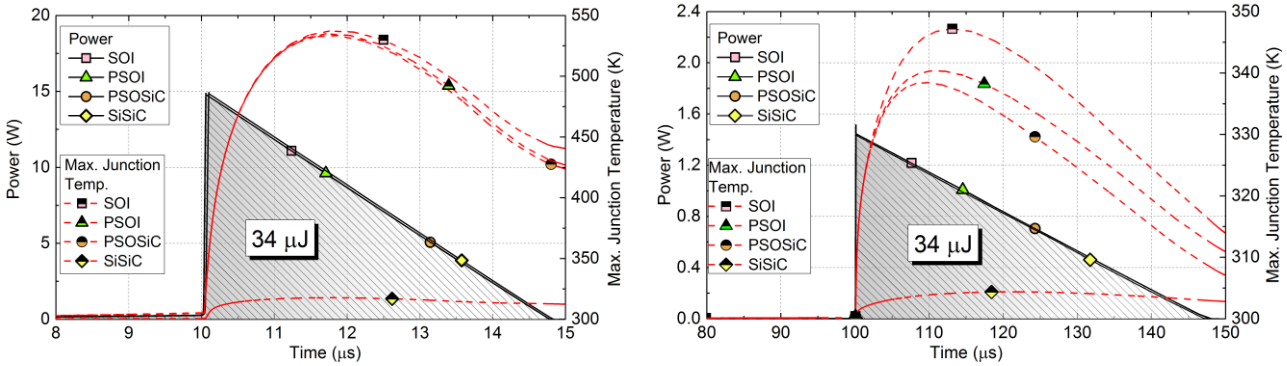

Fig.5. The power and temperature curves of inductive switching, under (left) the conditions mentioned in Fig. 4, and (right) with the inductor value and ramp-up time changed to 500 mH and 100 µs.

Conclusions

Simulations of inductive and capacitive switching are performed for a Si/SiC, SOI, PSOI and PSOSiC 190 V LDMOSFET. Through comparisons, the SOI group has the same electrical resistance at 300 K, which is lower than that of the Si/SiC. They also have similar transient thermal behaviour with power pulse lengths of 60 ns and 4.8 µs. When a 48-µs-pulse is used, the cooling effect of the thermal shunt network and SiC substrate in the PSOSiC is noticeable, but not strong enough to compete with the Si/SiC having maximum junction temperature close to 300 K in all simulated switching conditions. This indicates that the Si/SiC structure has much stronger energy capability than the SOI solutions, which is advantageous to high frequency and power applications.

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